AMENDMENT TO THE SPECIFICATION

Please replace paragraphs [0032] –[[0034] of the specification with the following amended paragraphs [0032] – [0034]:

[0032] After cleaning, a first dose (e.g., a high dose) of nitrogen is introduced as shown in FIG. 3. Various techniques may be employed for nitridation in accordance with the principles of the invention. For example, the entire structure may receive a high concentration of nitrogen in the range of 8×10^{14} to 1×10^{22} ~~atoms/centimeter~~ atoms/cm^3, after which, areas warranting a low concentration of nitrogen may be stripped of the concentrated nitrogen containing layer and then subjected to a low dose of nitrogen.

[0033] Nitrogen may be introduced by subjecting the device to a nitrogen containing gas such as ammonia (NH_3). The exposure introduces a first amount of nitrogen (e.g., a relatively high concentration) into the dielectric. During the time in which the substrate is exposed to the gas, an annealing process may be carried out. The annealing process may take place using a conventional furnace process or a rapid thermal process. The annealing conditions may include a temperature within the range of about 400°C. to 800°C., a pressure of 10 torr to 1 atmosphere, and an annealing time of 15 seconds to 120 minutes depending upon the type of process. The duration, temperature and pressure may be varied to increase or decrease the amount of nitrogen introduced in the dielectric. By way of example, and not limitation, a nitridation step according to the annealing conditions described above may produce a layer with a high concentration of nitrogen in the range of 8×10^{14} to 1×10^{22} ~~atoms/centimeter~~ atoms/cm^3. However, other levels of nitrogen concentration may be achieved. Indeed, various nitrogen levels may be desired, based upon the type of corresponding device, subsequent processing conditions, the gate oxide dielectric, doped semiconductor layer, and the concentration of the p_+ impurity formed within doped semiconductor layer. It is the added nitrogen which prevents p-type dopant impurities (for example Boron) from diffusing into the gate dielectric film and further diffusing into the channel region of the semiconductor structure. The presence of nitrogen also reduces current leakage. Upon completing this step, an oxynitride layer 310 formed near the substrate 110 interface of

the dielectric layer 120. A nitride (e.g., Si_3N_4) layer forms over areas 320 and 330 from which the dielectric was removed.

[0034] Next, the nitride is removed from areas that will not benefit from the first dose of nitrogen. For example, if the first dose is configured to impart a relatively high concentration of nitrogen (e.g., greater than 8 x 10^{14} ~~atoms/cm~~ atoms/cm^3), then the dielectric may be removed from areas designed to accommodate pFETs, such as for example area 330. As nFETs with thin gate dielectric layers benefit substantially from a relatively high concentration of nitrogen (e.g., greater than 8 x 10^{14} ~~atoms/cm~~ atoms/cm^3), the dielectric may be left in those areas, such as for example 320. Nitrogen-enriched dielectric may also be left in areas corresponding to a relatively thick gate dielectric, such as 120, though the impact of nitrogen in such areas may be rather muted. The removal from area 330 may be accomplished in a conventional manner using techniques known in the art, such as by masking and etching. A photoresist mask 410, as shown in FIG. 4, may cover areas 120 and 320. By way of example, a buffered hydrofluoric acid (BHF) may be used to etch away the nitride from area 330.

Please replace paragraph [0036] of the specification with the following amended paragraph [0036]:

[0036] After removal of the mask, the entire unmasked surface may be subjected to another dose of nitrogen, such as by exposing the structure to a nitrogen containing gas such as ammonia (NH_3), as shown in FIG. 6. This exposure forms a thin nitride (Si_3N_4) film 610 on exposed substrate, ~~34~~ introduces additional nitride on layer 320 and introduces a second amount of nitrogen into the dielectric area 310. During the time in which the structure is exposed to the gas, an annealing process is carried out. The annealing process may take place using a conventional furnace process (i.e., furnace nitridation) or a rapid thermal process (i.e., rapid thermal nitridation). The annealing conditions may include a temperature within the range of about 400°C. to 800°C., a pressure of 10 torr to 1 atmosphere, and an annealing time of 15 seconds to 120 minutes depending upon the type of process. The duration, temperature and pressure may be varied to increase or decrease the amount of nitrogen introduced. By way of

example and not limitation, a nitridation step according to the conditions described above may add nitrogen in the range of 1 x 10^{13} to 1 x 10^{15} ~~atoms/centimeter~~ atoms/cm^3 (e.g., 1 x 10^{14} to 1 x 10^{15} ~~atoms/centimeter~~ atoms/cm^3). The thickness of nitride file 610 may be approximately 10 to 50 Å. However, other levels of nitrogen concentration and other film thicknesses may be achieved.

Please replace paragraphs [0046] –[[0047] of the specification with the following amended paragraphs [0046] – [0047]:

[0046] Referring again to FIG. 11, the mask 1130 may mask those areas of the structure which are to become pFET regions 1150, and expose those portions of the structure which are to become nFET regions 1140. Nitrogen may be implanted through sacrificial oxide layer 1110 into underlying unmasked wells 1140 for n-FET regions. Sacrificial oxide layer 1110 attenuates the implantation so that the majority of implanted nitrogen atoms form a nitrogen enriched area at the well surface 1140. Mask 1130 prevents area 1150 from being implanted with nitrogen while area 1140 is implanted with nitrogen. A high dose of implanted nitrogen may yield approximately 8 x 10^{14} to 1 x 10^{22} ~~atoms/centimeter~~ atoms/cm^3 in the well. After implantation, the mask 1130 is stripped using well known techniques.

[0047] Optionally, nitrogen may also be implanted in n-wells (e.g., well 1150) for p-FET regions. Referring now to FIG. 12, mask 1230 is formed to mask those areas of the structure which are to become nFET regions 1140, and expose those portions of the structure which are to become pFET regions 1150. Alternatively, as nFETs benefit from high nitrogen concentrations, mask 1230 may be omitted. Nitrogen may be implanted through sacrificial oxide layer 1110 into underlying unmasked areas. Sacrificial oxide layer 1110 attenuates the implantation so that the majority of implanted nitrogen atoms form a nitrogen enriched area at the well surfaces 1150. For pFETs, a low dose of implanted nitrogen may yield approximately 1 x 10^{13} to 1 x 10^{15} ~~atoms/centimeter~~ atoms/cm^3 in the well. After implantation, the mask 1230, if any, is stripped using well known techniques. Optionally, a rapid thermal anneal (e.g., 1050° C. for 30 seconds) may be performed to diffuse implanted nitrogen.